IN THE CLAIMS

This listing of claims replaces all prior listings:

1. (Currently Amended) A display apparatus comprising:

a pixel array unit including pixels arranged in a matrix and signal lines arranged so that one corresponds to each vertical column of pixels in the matrix of pixels;

a clock generating unit for generating a horizontal start pulse for indicating a start of horizontal scanning, first clock pulses being used as a basis for the horizontal scanning, and second clock pulses having n phases and being synchronized with the first clock pulses, where n is an integer equal to or greater than three;

a shift register including cascaded shift register stages for sequentially transferring the horizontal start pulse in synchronism with the first clock pulses, the shift register being configured to successively output transfer pulses from the shift register stages;

a group of first switches configured to successively generate sampling pulses by extracting the second clock pulses in response to the transfer pulses successively output from the shift register; and

a group of second switches configured to successively sample input video signals in response to the sampling pulses generated by the group of first switches and to provide the video signals to the signal lines in the pixel array unit,

wherein,

the start pulse has a pulse width that includes a plurality of pulse widths of the first clock pulses, and

the group of second switches are divided into at least two subgroups including a first subgroup of nonadjacent second switches and a second subgroup of second switches arranged next to the second switches in the first subgroup, the video signals are divided into at least two signal groups and then provided to the at least two subgroups of second switches, respectively, and the sampling pulses generated by the group of first switches are divided and provided to the at least two subgroups of switches in the group of second switches.

2. (Original) The display apparatus according to claim 1, wherein a pulse interval of the second clock pulses is n times a pulse interval of the first clock pulses, where n is an integer equal to or larger than three.

3. (Original) The display apparatus according to claim 2, wherein a pulse width of each of the second clock pulses is larger than a pulse width of each of the first clock pulses.

4. (Cancelled)

5. (Currently Amended) The display apparatus according to claim [[4]] 1, wherein a pulse interval of the second clock pulses is n times a pulse interval of the first clock pulses, where n is an integer equal to or larger than three.

6. (Previously Presented) The display apparatus according to claim 5, wherein a pulse width of each of the second clock pulses is larger than a pulse width of each of the first clock pulses.

7. (Original) The display apparatus according to claim 1, wherein electrooptic elements in the pixels are liquid crystal cells.

8. (Currently Amended) The display apparatus according to claim 6, wherein the group of second switches are divided into at least two subgroups including a first subgroup of nonadjacent second switches and a second subgroup of second switches arranged next to the second switches in the first subgroup, the video signals are divided into at least two ~~systems~~ signal groups and then provided to the at least two subgroups of second switches, and the sampling pulses generated by the group of first switches are divided and provided to the at least two subgroups of switches in the group of second switches.

9. (Currently Amended) A method for driving a display apparatus, the display apparatus comprising:

a pixel array unit including pixels arranged in a matrix and signal lines arranged so that one corresponds to each vertical column of pixels in the matrix of pixels;

a clock generating unit for generating a horizontal start pulse for indicating a start of horizontal scanning, first clock pulses being used as a basis for the horizontal scanning, and second clock pulses having n phases and being synchronized with the first clock pulses, where n is an integer equal to or greater than three;

a shift register including cascaded shift register stages for sequentially transferring the horizontal start pulse in synchronism with the first clock pulses, the shift register being configured to successively output transfer pulses from the shift register stages;

a group of first switches configured to successively generate sampling pulses by extracting the second clock pulses in response to the transfer pulses successively output from the shift register; and a group of second switches configured to successively sample input video signals in response to the sampling pulses generated by the group of first switches and to provide the video signals to the signal lines in the pixel array unit,

wherein,

the start pulse has a pulse width that includes a plurality of pulse widths of the first clock pulses, and

the group of second switches are divided into at least two subgroups including a first subgroup of nonadjacent second switches and a second subgroup of second switches arranged next to the second switches in the first subgroup, the video signals are divided into at least two signal groups and then provided to the at least two subgroups of second switches, respectively, and the sampling pulses generated by the group of first switches are divided and provided to the at least two subgroups of switches in the group of second switches.

10. (Original) The method of driving the display apparatus according to claim 9, wherein a pulse interval of the second clock pulses is n times a pulse interval of the first clock pulses, where n is an integer equal to or larger than three.

11. (Original) The method of driving the display apparatus according to claim 9, wherein a pulse width of each of the second clock pulses is larger than a pulse width of each of the first clock pulses.